REMARKS

Claims 1, 6, 9, 10 and 14 are pending in the present application. Claims 1 and 9 have been amended. Claims 2, 5, 7, 8 and 11-13 have been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the Priority document.

Claim Rejections – 35 U.S.C. 103

Claims 1, 5, 6, 9-11, 13 and 14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Chiu et al. reference (U.S. Patent No. 4,514,897) in view of the Fujii et al. reference (U.S. Patent No. 5,017,979). This rejection is respectfully traversed for the following reasons.

The method of manufacturing a non-volatile semiconductor storage device of claim 1 includes in combination "a first step of successively forming a first insulating film and a first polysilicon layer on a semiconductor substrate, and implanting nitrogen ions into a front surface of the first polysilicon layer"; "a second step of patterning a first polysilicon layer and a first insulating film into the shape of a band"; and "a third step of thermally oxidizing the patterned band-shaped first polysilicon layer, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof;...wherein the nitrogen ions are implanted into the first polysilicon layer so as to be located only in the front surface of the first polysilicon layer". Applicant respectfully submits that the method of manufacturing a nonvolatile

semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner.

As emphasized beginning on page 11 of the Amendment dated August 5, 2005, the Chiu et al. reference as relied upon by the Examiner does not specifically describe that silicon dioxide layer 24 as shown in Fig. 2 is thicker at side surfaces of floating gate 13 than at a front surface of floating gate 13. As described in column 6, line 60-66 of the Chiu et al. reference with respect to Fig. 5d, silicon dioxide layer 24 is grown on the first level polysilicon, producing a coating on all exposed surfaces of the poly including tops and sides. Silicon dioxide layer 24 is grown at about 1100°C in O_2 for about 55 minutes and in N_2 for 30 minutes, "producing about 1200 Å thickness and consuming part of the polysilicon". There is no specific description pertaining to different respective silicon dioxide layer thicknesses.

In the Response to Arguments section on page 7 of the Final Office Action dated May 17, 2006, the Examiner has asserted that:

> "As shown in Fig. 2, the silicon oxide layer 24 **appears** thicker in bottom edge surface of the floating gate 13 than the top surface of floating gate 13. In addition, in the absence of specification thickness range of the silicon oxide layer on the top surface relative to the sidewall surface of the floating gate applicant's own drawings are not drawn to scale" (our emphasis added).

Applicant however respectfully submits that in absence of specific description in the Chiu et al. reference that silicon dioxide layer 24 is thicker on side surfaces of poly

13 than on a front surface thereof, and/or reasoning as offered by the Examiner that would specifically establish why silicon dioxide layer 24 would be formed thicker on side surfaces of poly 13 in view of the processing parameters as set forth in the Chiu et al. reference, it must be considered that any perceived difference in thickness of silicon dioxide layer 24 in Figs. 2 and 7 of the Chiu et al. reference is merely incidental. Particularly, silicon dioxide layer 24 of the Chiu et al. reference would appear to be substantively conformal.

As described beginning on page 7, line 9 of the specification of the present application with respect to Fig. 3A, nitrogen ions (N) are implanted into the front surface of polysilicon layer 14A so as to stay only in the front surface. The implantation conditions of nitrogen ions are therein described. As further described beginning on page 8, of the Chiu et al. reference, during the corresponding thermal oxidation, since the front surface of polysilicon layer 14B has been implanted with nitrogen ions, the growth of the oxide film is slower at the front surface of polysilicon layer 14B than at side surfaces thereof where no nitrogen ions exist. As subsequently described, inter-gate insulating film 15a in Fig. 3C of the Chiu et al. reference is therefore about 10nm thick on the front surface of polysilicon layer 14B, and inter-gate insulating film 15b is about 12-20nm thick on side surfaces of polysilicon layer 14B and tunnel oxide film 13.

Accordingly, contrary to the Examiner's assertion on page 7 of the Final Office Action, thickness ranges of the silicon oxide layer on top and side surfaces of the polysilicon layer are described, and the thickness of inter-gate insulating layers 15a and 15b in Figs. 3A-3E of the present application may be perceived to be relatively to scale.

The Examiner has further asserted on page 7 of the Final Office Action that "Limitations appearing in the specification but not recited in the claim are not read into the claim". This position as taken by the Examiner is not entirely understood, because claim 1 clearly features "a third step of thermally oxidizing the patterned band-shaped first polysilicon layer, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof".

With further regard to this rejection, the Examiner has apparently interpreted barrier layer 43 in Fig.14A of the Fuji et al. reference as the implanted nitrogen ions of the claims. However, as asserted beginning on page 13 of the Amendment dated August 5, 2005, barrier layer 43 in Fig. 14A of the Fujii et al. reference is not implanted into polysilicon film 42 so as to be located only in the front surface of polysilicon film 42, as would be necessary to meet the features of current claim 1. Particularly, barrier layer 43 in Fig. 14A of the Fujii et al. reference is locally implanted into the polysilicon film 42 appreciably below the surface of polysilicon film 42. Barrier layer 43 is not located at the surface of polysilicon film 42. The Fujii et al. reference as relied upon thus does not overcome the deficiencies of the Chiu et al. reference.

Applicant therefore respectfully submits that the method of manufacturing a nonvolatile semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 1 and 6, is improper for at least these reasons. The Examiner is respectfully requested to take note of this traversal as initially presented in the Amendment dated August 5, 2005, and to answer the substance of it on the record.

The method of manufacturing a semiconductor device of claim 9 features in combination "implanting nitrogen ions into a front surface of the first polysilicon layer"; "thermally oxidizing the band-shape segment to simultaneously grow the second insulating film on side surfaces and the front surface of the first polysilicon layer, wherein the second insulating film is grown thicker on the side surfaces of the first polysilicon layer than on the front surface of the polysilicon layer implanted with nitrogen ions;...wherein said implanting nitrogen ions is performed prior to said patterning the first insulating film and the first polysilicon layer, and wherein the nitrogen ions are implanted into the first polysilicon layer so as to be located only in the front surface of the first polysilicon layer".

Applicant respectfully submits that the prior art as relied upon by the Examiner, particularly the Chiu et al. reference, does not disclose a second insulating film that is thicker on side surfaces of a first polysilicon layer than on a front surface of a polysilicon layer implanted with nitrogen ions. Moreover, the prior art as relied upon by the Examiner does not disclose or make obvious nitrogen ions which are implanted into a first polysilicon layer so as to be located only in a front surface of the first polysilicon layer, as will be necessary to meet the further features of claim 9. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 9, 10 and 14, is improper for at least these reasons.

Conclusion

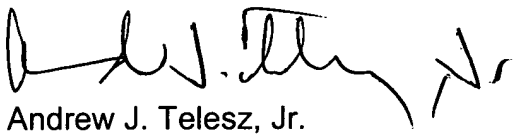
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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